AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An integrated circuit having a microprocessor comprising:

a field programmable gate array (FPGA) including a plurality of configurable logic blocks;

a configurable portion comprising one of a plurality of microcode sets, wherein each of the plurality of microcode sets is associated with a different set of macroinstructions;

a datapath unit coupled to at least one configurable logic block of the FPGA, the datapath unit configured to execute each different set of macroinstructions; and

a non-configurable portion comprising sequencing logic that is the same for each one of the plurality of microcode sets.

Claims 2-3. (Cancelled)

4. (Original) The integrated circuit of claim 1 wherein each microcode set of the plurality of microcode sets is associated with a microprocessor of a plurality of microprocessors.

5. (Cancelled)

6. (New) The integrated circuit of claim 4, wherein:

each different set of macroinstructions is associated with a different microprocessor of the plurality of microprocessors; and

the datapath unit includes an arithmetic logic unit, and the arithmetic logic unit is adapted to execute all arithmetic and logic operations in the microcode sets associated with the plurality of microprocessors.